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	U. S. P.	ATENTS & P.	ATENT APPL	ICATION PUBL	ICATIONS				
	Document Number	Date	Name		Class	Subclass	Filing Date if Appropriate		
1	6,539,072	03-25-03	Donnelly et al.		375	371			
<u> </u>		09-26-00	Donnelly et al.		375	371			
		03-25-97	Lee et al.		327	158			
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	OTHER DO	OCUMENTS (Including Aut	hor, Title, Date, I	Pertinent Page	es, Etc.)			
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	Pater OF DO (Us	Patent and Trademark Copy Document Number Document Number	Patent and Trademark Office OF DOCUMENTS CITED BY APPLICATION (Use several sheets if necessary) U. S. PATENTS & P Document Number 1 6,539,072 03-25-03 2 6,125,157 09-26-00 3 5,614,855 03-25-97 4 5,485,490 5,485,490 FORE Document Number Date OTHER DOCUMENTS	Patent and Trademark Office OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary) U. S. PATENTS & PATENT APPL Document Number Date 1 6,539,072 03-25-03 Donnelly et a 2 6,125,157 09-26-00 Donnelly et a 3 5,614,855 03-25-97 Lee et al. 4 5,485,490 5,485,490 Leung et al. FOREIGN PATENT Document Number Date OTHER DOCUMENTS (Including Aut	Patent and Trademark Office OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary) Applicants: I Filing Date: U. S. PATENTS & PATENT APPLICATION PUBL Document Number Date Name 1 6,539,072 03-25-03 Donnelly et al. 2 6,125,157 09-26-00 Donnelly et al. 3 5,614,855 03-25-97 Lee et al. 4 5,485,490 5,485,490 Leung et al. FOREIGN PATENT DOCUMENTS Document Number Date Country OTHER DOCUMENTS (Including Author, Title, Date, I	Document Number Date Name Class	Patent and Trademark Office		

EXAMINER *EXAMINER DATE CONSIDERED

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FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office				Attorney Docket Number 5646-113			Serial No. 10/648,090			
LIST OF DOCUMENTS CITED BY APPLICANT										
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M 1	1	IDT Clock Management Products Family, 8/2002, Admitted Prior Art, 4 pages								
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Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office LIST OF DOCUMENTS CITED BY APPLICANT					Attorney Docket Number 5646-113			Serial No. To Be Assigned	
(Use several sheets if necessary)					Applicants: Declan McDonagh et al.				
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		U. S. P	ATENTS & P	ATENT APPL	ICATION PUBI	ICATIONS			
Examiner Initial		Document Number	Date	Name		Class	Subclass	Filing Date if Appropriate	
W.	1	6,597,212	7/22/03	Wang et al.		327	117		
M	2	6,525,584	2/25/03	Seo et al.		327	276		
1	3	6,509,773	1/21/03	Buchwald et al.		327	248		
	4	6,466,098	10/15/02	Pickering		331	25		
	5	6,433,645	8/13/02	Mann et al.		331	18		
	6	6,388,478	5/14/02	Mann		327	113		
	7	6,384,653	5/7/02	Broome		327	247		
	8	6,359,486	3/19/02	Chen		327	231		
	9	6,329,859	12/11/01	Wu		327	291		
4	10	6,271,702	8/7/01	Stansell		327	295		
M	11	6,111,445	8/29/00	Zerbe et al.		327	231		
					<i>`</i>				
	•		FORE	IGN PATENT	DOCUMENTS				
		Document Number	Date	Country		Class	Subclass	Translation Yes No	
					1				
		OTHER DO	CUMENTS (I	ncluding Autho	or, Title, Date, Po	ertinent Pages	s, Etc.)		
	12_	Rabaey, Jan M., "Synchronization at the System Level," Digital Integrated Circuits, A Design Perspective, Prentice-Hall, Inc., pp. 540-543 NO DATE IS PRIVING							
M	13	"High Speed Multi-Phase PLL Clock Buffer," Cypress Semiconductor Corporation, Revised July 25, 2003, 14 pages							

EXAMINER *EXAMINER

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DATE CONSIDERED

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Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.